Claims

1. A method for fabricating a three-dimensional integrated device including a plurality of vertically stacked and interconnected wafers, the method comprising the steps of:

providing a first wafer (1) having a front surface (1a) and a back surface (1b), the first wafer having devices formed in a region (1d) adjacent to the front surface thereof;

forming a via (12) in the first wafer extending from the front surface, the via being characterized by a lateral dimension (121) at the front surface;

removing material from the first wafer at the back surface (1b) thereof;

forming an opening (13) in the back surface of the first wafer, thereby exposing the via, the opening having a lateral dimension greater than said lateral dimension of the via;

forming a layer of conducting material (14) in said opening;

providing a second wafer (2) having a front surface (2a) and a back surface (2b), the second wafer having devices formed therein adjacent to the front surface thereof;

forming a stud (27) on the front surface of the second wafer;

forming a layer of bonding material (26) on the front surface (2a) of the second wafer, the studs projecting vertically therefrom;

aligning the stud (27) to the opening (13) in the back surface of the first wafer; and

bonding the second wafer to the first wafer using the layer of bonding material (26), so that the stud makes electrical contact with the via.

2. A method according to claim 1, further comprising the steps of:

forming a via (22) in the second wafer (2) extending from the front surface thereof (2a), the via being characterized by a lateral dimension (221) at the front surface (2a);

removing material from the second wafer at the back surface (2b) thereof;

forming an opening (23) in the back surface (2b) of the second wafer, thereby exposing the via (22) therein, said opening (23) having a lateral dimension greater than said lateral dimension (221) of the via (22);

forming a layer of conducting material (24) in said opening;

providing a third wafer (3) having a front surface (3a), the third wafer having devices formed therein adjacent to the front surface thereof;

forming a stud (37) on the front surface (3a) of the third wafer;

forming a layer of bonding material (36) on the front surface (3a) of the third wafer, the studs projecting vertically therefrom;

aligning the stud (37) to the opening (23) in the back surface of the second wafer; and

bonding the third wafer to the second wafer using the layer of bonding material (36), so that the stud (37) of the third wafer makes electrical contact with the via (22) of the second wafer, with the stud (27) of the second wafer, and with the via (12) of the first wafer.

3. A method according to claim 1 or claim 2, characterized in that said step of removing material causes the wafer to have a thickness of less than 20μm.

4. A method according to claim 1 or claim 2, further comprising the step of attaching a handling plate (15) to the front surface (1a) of the first wafer (1) using a layer of bonding material (16).

5. A method according to any preceding claim, further comprising the step of forming a conducting body (102) in one of the first wafer (1) and the second wafer (2) and connecting to the via (12/22) in the wafer, the conducting body extending laterally under the devices of the wafer, and characterized in that the opening (103) in the back side of the wafer is separated laterally from the via in accordance with the lateral extent of the conducting body (102).

6. A method according to any preceding claim, further comprising the steps of:

forming an additional opening (113) in the back surface of the first wafer;

forming an additional layer of conducting material (114) in said additional opening;

forming an additional stud (127) on the front surface of the second wafer; and

aligning the additional stud (127) to the additional opening (113) in the back surface of the first wafer;

and characterized in that said step of bonding the second wafer to the first wafer forms a connection between the additional stud (127) and the additional layer of conducting material (114) for conducting heat between the second wafer and the first wafer.

7. A method according to claim 6, characterized in that the additional layer of conducting material (114) is electrically insulated from the via (12).

8. A method according to claim 2, further comprising the steps of:

forming an additional opening in the back surface of the second wafer;

forming an additional layer of conducting material in said additional opening;

forming an additional stud on the front surface of the third wafer; and

aligning the additional stud to the additional opening in the back surface of the second wafer;

and characterized in that said step of bonding the third wafer to the second wafer forms a connection between the additional stud and the additional layer of conducting material for conducting heat between the third wafer and the second wafer.

9. A method according to any preceding claim, characterized in that said bonding material is a thermoplastic material.

10. A method according to claim 9, characterized in that the thermoplastic material is polyimide.

11. A method according to any of claims 1-10, further comprising the step of attaching the three-dimensional integrated device (100) to a multichip module (300).

12. A method according to any of claims 1-10, further comprising the step of attaching the three-dimensional integrated device (401) to an insulating layer having wiring formed therein (450) using a stud-via connection.

13. A method according to any of claims 2-12, characterized in that the first wafer and second wafer have cache memory devices, and the third wafer has logic devices.

14. A method according to any of claims 2-12, characterized in that at least one of the first wafer, the second wafer and the third wafer includes a MEMS device.

AMENDED CLAIMS
[received by the International Bureau on 08 July 2003 (08.07.03);
original claims 5, 6, 9 and 11-14 amended]

forming a layer of conducting material (24) in said opening;

providing a third wafer (3) having a front surface (3a), the third wafer having devices formed therein adjacent to the front surface thereof;

forming a stud (37) on the front surface (3a) of the third wafer;

forming a layer of bonding material (36) on the front surface (3a) of the third wafer, the studs projecting vertically therefrom;

aligning the stud (37) to the opening (23) in the back surface of the second wafer; and

bonding the third wafer to the second wafer using the layer of bonding material (36), so that the stud (37) of the third wafer makes electrical contact with the via (22) of the second wafer, with the stud (27) of the second wafer, and with the via (12) of the first wafer.

3. A method according to claim 1 or claim 2, characterized in that said step of removing material causes the wafer to have a thickness of less than 20μm.

4. A method according to claim 1 or claim 2, further comprising the step of attaching a handling plate (15) to the front surface (1a) of the first wafer (1) using a layer of bonding material (16).

5. A method according to claim 1 or claim 2, further comprising the step of forming a conducting body (102) in one of the first wafer (1) and the second wafer (2) and connecting to the via (12/22) in the wafer, the conducting body extending laterally under the devices of the wafer, and characterized in that the opening (103) in the back side of the wafer is separated laterally from the via in accordance with the lateral extent of the conducting body (102).

6. A method according to claim 1 or claim 2, further comprising the steps of:

forming an additional opening (113) in the back surface of the first wafer;

forming an additional layer of conducting material (114) in said additional opening;

forming an additional stud (127) on the front surface of the second wafer; and

aligning the additional stud (127) to the additional opening (113) in the back surface of the first wafer;

and characterized in that said step of bonding the second wafer to the first wafer forms a connection between the additional stud (127) and the additional layer of conducting material (114) for conducting heat between the second wafer and the first wafer.

7. A method according to claim 6, characterized in that the additional layer of conducting material (114) is electrically insulated from the via (12).

8. A method according to claim 2, further comprising the steps of:

forming an additional opening in the back surface of the second wafer;

forming an additional layer of conducting material in said additional opening;

forming an additional stud on the front surface of the third wafer; and

aligning the additional stud to the additional opening in the back surface of the second wafer;

and characterized in that said step of bonding the third wafer to the second wafer forms a connection between the additional stud and the additional layer of conducting material for conducting heat between the third wafer and the second wafer.

9. A method according to claim 1 or claim 2, characterized in that said bonding material is a thermoplastic material.

10. A method according to claim 9, characterized in that the thermoplastic material is polyimide.

11. A method according to claim 1 or claim 2, further comprising the step of attaching the three-dimensional integrated device (100) to a multichip module (300).

12. A method according to claim 1 or claim 2, further comprising the step of attaching the three-dimensional integrated device (401) to an insulating layer having wiring formed therein (450) using a stud-via connection.

13. A method according to claim 2, characterized in that the first wafer and second wafer have cache memory devices, and the third wafer has logic devices.

14. A method according to claim 2, characterized in that at least one of the first wafer, the second wafer and the third wafer includes a MEMS device.